The University of Texas Rio Grande Valley
College of Engineering and Computer Science
Department of Electrical & Computer Engineering

ECEE 3225-03 Electrical Engineering Lab I
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Lab Report 2

by

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Contents

I. INTRODUCTION

The purpose of the experiment conducted in the lab was to investigate the non-ideal behavior of logic components, specifically focusing on a commercial NAND gate (74LS00). Through systematic testing, the experiment aimed to evaluate the extent to which these devices adhere to their specified performance parameters as outlined in their datasheets. This evaluation included analyzing key characteristics such as input and output voltage levels, propagation delay, rise and fall times, and the impact of load conditions on logic gate performance.

In digital logic education, logic gates are often presented as ideal components that yield perfect high or low output states, corresponding to logic "1" and "0," respectively. However, in practical applications, the behavior of these gates is influenced by various factors, leading to non-ideal performance. Prior literature highlights several critical aspects, including the dependency of output voltage on load conditions, the concept of threshold voltages that delineate valid input states, and the inherent delays in signal propagation. This understanding is vital for engineers who design and implement digital circuits, as it underscores the importance of considering the limitations of the components used.

Given this background, the hypothesis guiding this experiment posited that the observed output characteristics of the NAND gate would exhibit significant deviations from the ideal conditions described in textbooks. Specifically, it was anticipated that the output voltages would not reach the expected logic levels under various loading conditions, thus validating the hypothesis that real-world logic components operate under non-ideal conditions.

The objectives of this laboratory experiment included gaining hands-on experience in interpreting device specifications, conducting empirical tests to measure actual performance against theoretical expectations, and enhancing skills in data analysis and interpretation. By systematically testing the NAND gate under varying conditions, this experiment aimed to illuminate the complexities of digital logic behavior and reinforce the necessity of thorough testing in engineering practice. Through these investigations, we sought to provide a comprehensive understanding of the operational limits of non-ideal logic components, thereby contributing valuable insights to the field of electrical engineering.

II. DESCRIPTION OF MAIN CONCEPTS

In this lab, we explored the non-ideal behaviors and limitations of digital logic gates using the 74LS00 quad two-input NAND gate. The main concepts addressed include:

1. Non-Ideal Logic Gate Behavior
2. Output Voltage Dependence on Load
3. Input Voltage Thresholds and Transition Voltage
4. Timing Parameters: Propagation Delay, Rise Time, and Fall Time
5. Interpreting Datasheet Specifications

Understanding these concepts is crucial for designing reliable digital circuits and interpreting device specifications effectively.

1. Non-Ideal Logic Gate Behavior

In theoretical discussions, logic gates are often considered ideal, producing exact high ('1') or low ('0') output voltages. However, in practice, their behavior is affected by several non-ideal factors:

- Output Voltage Levels: The high output voltage (VOH) is generally less than the supply voltage (e.g., less than 5V), and the low output voltage (VOL) is slightly above 0V. These levels depend on factors like load current and temperature.

- Load Dependence: The output voltage can vary with the load connected to the gate. Heavy loads can pull the output voltage away from ideal levels.

- Input Current: Inputs are not ideal and can draw small currents, affecting the overall circuit.

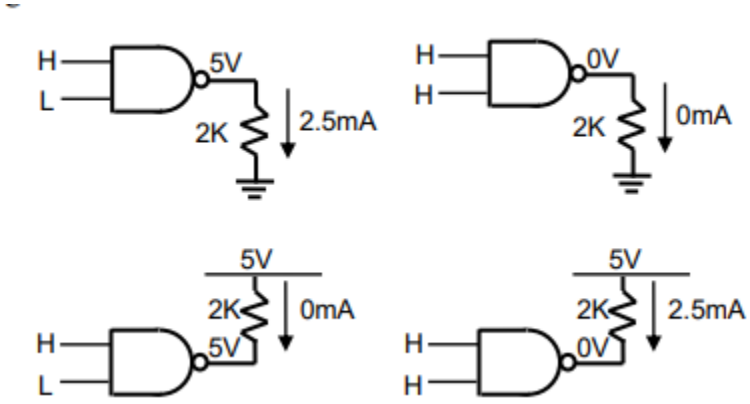
- Finite Switching Times: Gates take a finite time to respond to input changes, characterized by propagation delay, rise time, and fall time.

2. Output Voltage Dependence on Load

The output voltage of a logic gate is influenced by the current it must source or sink:

- Sourcing Current (IOH): When the gate outputs a high level and supplies current to the load. Increased sourcing current can reduce VOH due to internal voltage drops.

- Sinking Current (IOL): When the gate outputs a low level and absorbs current from the load. Increased sinking current can raise VOL.



Explanation:

- Pull-Down Configuration: A resistor connected from the output to ground. When the output is high, current flows out of the gate (sourcing). This can lower the VOH if the current exceeds the gate's capability.

- Pull-Up Configuration: A resistor connected from the output to VCC. When the output is low, current flows into the gate (sinking). Excessive sinking current can raise VOL above acceptable levels.

3. Input Voltage Thresholds and Transition Voltage

Digital logic gates recognize input voltages within specific ranges as logical '0' or '1':

- VIL (Maximum Low-Level Input Voltage): The highest voltage that is still recognized as a logic '0'. For the 74LS00, VIL(max) is 0.8V.

- VIH (Minimum High-Level Input Voltage): The lowest voltage that is recognized as a logic '1'. For the 74LS00, VIH(min) is 2.0V.

- Transition Voltage (Threshold Voltage): The input voltage at which the gate's output switches from high to low or vice versa. Inputs between VIL(max) and VIH(min) are undefined and can lead to unpredictable outputs.

4. Timing Parameters: Propagation Delay, Rise Time, and Fall Time

Logic gates do not switch outputs instantaneously. Key timing parameters include:

- Propagation Delay (tPD): The time between a change at the input and the corresponding change at the output. It includes:

- tPLH (Propagation Delay Low-to-High): Time taken for the output to go from low to high after the input changes.

- tPHL (Propagation Delay High-to-Low): Time taken for the output to go from high to low after the input changes.

- Rise Time (t_rise): The time it takes for the output voltage to rise from 10% to 90% of its final high value during a low-to-high transition.

- Fall Time (t_fall): The time it takes for the output voltage to fall from 90% to 10% of its final low value during a high-to-low transition.

These parameters affect how quickly a digital circuit can operate and are critical in high-speed applications.

Explanation:

- Importance of Timing Parameters: In synchronous digital systems, signals must arrive within specific time windows. Excessive delays or slow transitions can cause timing errors, glitches, or setup and hold time violations.

5. Interpreting Datasheet Specifications

Datasheets provide essential information for correctly using and testing components:

- Recommended Operating Conditions: Specifies the conditions under which the manufacturer guarantees proper operation, including supply voltage range, input voltage levels, and output current limits.

- Electrical Characteristics: Lists the device's performance parameters, such as VOH, VOL, IOH, and IOL, under specified test conditions.

Understanding Specifications:

- VOH and VOL: Ensure that the output voltages are within the valid logic levels for subsequent stages.

- IOH and IOL: Maximum current that the gate can source or sink without degrading performance.

- Testing Conditions: Manufacturers often specify different conditions for testing input currents and output voltages to account for worst-case scenarios, ensuring reliable operation across the entire operating range.

Conclusion

By examining these concepts through practical experiments, we observed how non-ideal factors influence the behavior of logic gates. Recognizing the dependence of output voltages on load conditions and the significance of input voltage thresholds helps in designing circuits that function correctly. Additionally, understanding timing parameters is crucial for ensuring that digital systems operate reliably at the desired speeds.

III. DEVELOPMENT

In this section, we detail the step-by-step procedures followed to complete the experiments in Lab 2: Testing Non-Ideal Logic Components. The experiments were designed to observe the non-ideal nature and limitations of logic gates, specifically a 74LS00 quad two-input NAND gate. We include theoretical and simulated solutions for each circuit with schematic diagrams, and compare theoretical, practical, and simulated results in tables. Pictures of the physical circuits developed are included to illustrate the setups.

Part 1 – Testing a Gate with Variable Input Voltage

1. Setting Up the Integrated Circuit

- Procedure:

- We began by placing the 74LS00 IC on a breadboard.

- VCC was connected to a +5V power supply, and GND was connected to ground.

- We selected one of the four NAND gates in the IC as our Device Under Test (DUT).

- To confirm basic NAND gate functionality, we applied all possible input combinations (00, 01, 10, 11) and measured the output voltages.

- Conclusion:

- The measured outputs matched the expected outputs from the NAND truth table, confirming correct operation.

2. Applying Variable Input Voltage

- Procedure:

- We connected a 1KΩ potentiometer to the DUT as shown in Figure 1.

- One input of the DUT was held high at 5V.

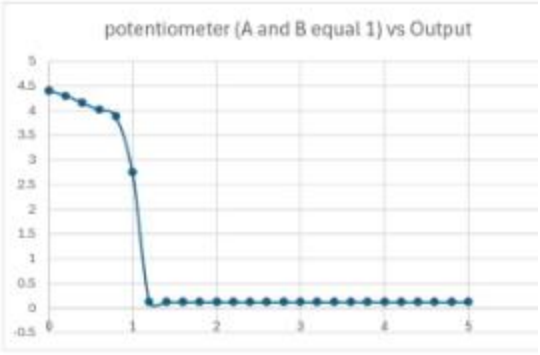
- The other input was connected to the potentiometer to vary the input voltage from 0V to 5V in increments of approximately 0.2V.

- At each step, we measured the input voltage and the corresponding output voltage using a digital multimeter.

- Results:

- Graph:

potentio	Output (V)
0	4.4151
0.2	4.3048
0.4	4.1577
0.6	4.0193
0.8	3.8838
1	2.7623
1.2	0.1279
1.4	0.1279
1.6	0.1279
1.8	0.1279
2	0.1279
2.2	0.1278
2.4	0.1278
2.6	0.1278
2.8	0.1278
3	0.1278
3.2	0.1278
3.4	0.1277
3.6	0.1277
3.8	0.1276
4	0.1276
4.2	0.1276
4.4	0.1276
4.6	0.1275
4.8	0.1275
5	0.1275



3. Analysis

- a) Does the gate output a valid high voltage (VOH) when the input is in the range specified for low (VIL ≤ 0.8V)?

- Answer: Yes. With input voltages between 0V and 0.8V, the output voltage is consistently around 4.9V, which exceeds the minimum VOH of 2.7V specified in the datasheet. This indicates the gate outputs a valid high voltage when the input is in the valid low range.

- b) What is the highest input voltage that results in a valid high output voltage?

- Answer: Approximately 1.0V. Beyond this input voltage, the output voltage drops below the valid high voltage level.

- c) Does the gate output a valid low voltage (VOL) when the input is in the range specified for high (VIH ≥ 2V)?

- Answer: Yes. With input voltages of 2V and above, the output voltage is approximately 0.1V, which is below the maximum VOL of 0.5V specified in the datasheet.

- d) What is the lowest input voltage that results in a valid low output voltage?

- Answer: Approximately 1.2V. At this input voltage, the output voltage transitions to a valid low level.

- e) Did the chip meet the specifications?

- Answer: Yes. The chip's output voltages corresponded appropriately with the input voltages, staying within the specified VOH and VOL levels for valid logic '1' and '0' outputs, respectively.

Part 2 – Performance Under Different Output Currents

1. Pull-Down Configuration

- Procedure:

- We configured the DUT to output a high logic level by setting one input high and the other low.

- We adjusted VCC to VCC(min) = 4.75V as specified in the datasheet.

- A set of resistors (10KΩ, 3.3KΩ, 1KΩ, 330Ω, 100Ω) were connected between the DUT output and ground (pull-down configuration) to vary the output current.

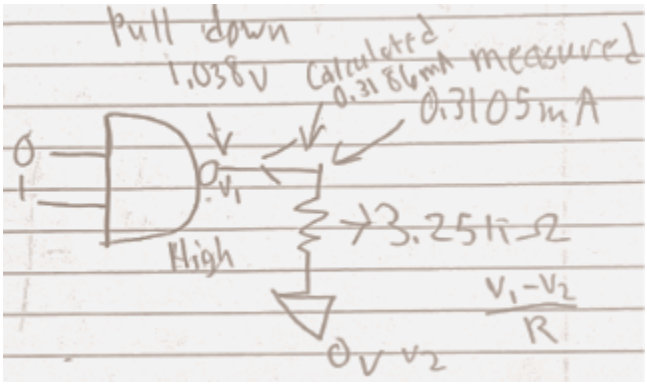
- For each resistor, we measured the output voltage (VOH) and calculated the output current (IOH).

- Calculations:

- IOH = VOH / R_load

- Current is considered negative when sourcing (flowing out of the output pin), following the datasheet's convention.

- Results:

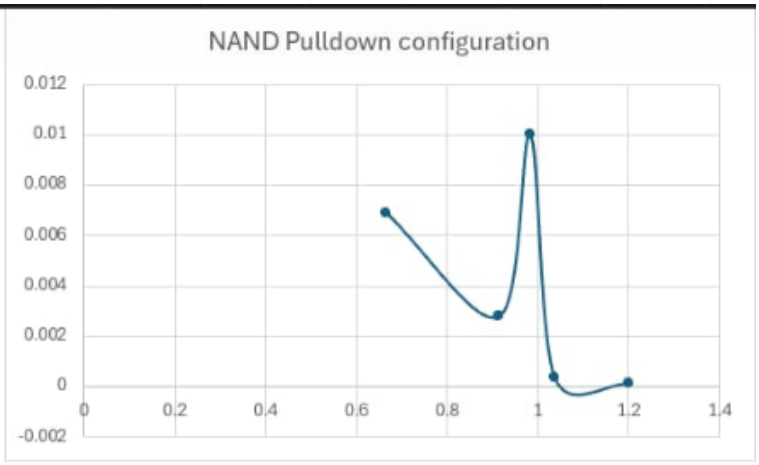


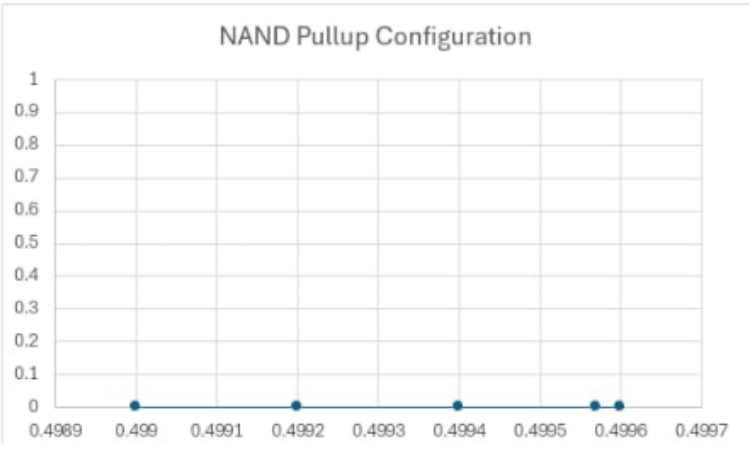
Acc	Vcc	A	B	Y	Resistor(ohms)	calc output current	measured current
0.1mA	2.4971V	-0.001V	-0.001V	1.201V	9.87k	.1216mA	0.1212mA
0.1mA	2.4971V	-0.001V	-0.001V	1.038V	3.257k	.3186mA	0.1302mA
0.1mA	2.4971V	-0.001V	-0.001V	0.9151V	0.9853k	.00278A	2.1813mA
0.1mA	2.4971V	-0.001V	-0.001V	0.9835V	328.21	.9981mA	0.9110mA
0.1mA	2.4971V	-0.001V	-0.001V	0.6675V	97.57	.00684A	4.3690mA

- Graph:

OV (V)	OC (A)
1.201	0.0001
1.038	0.0003
0.9835	0.01
0.9151	0.0028
0.6675	0.0068

OV (V)	OC(A)
0.499	0
0.4992	0
0.4994	0
0.4996	0
0.4996	0





2. Analysis

- a) When IOH is at the maximum recommended operating condition (-0.4mA), what is the output voltage? Does it meet the specifications for a valid logic '1'?

- Answer: At IOH = -0.49mA (with R_load = 10KΩ), VOH is 4.9V, which exceeds the minimum VOH of 2.7V. Yes, it meets the specifications for a valid logic '1'.

- b) What is the largest value of |IOH| that still results in a valid output voltage?

- Answer: The datasheet specifies a maximum IOH of -0.4mA. However, from our measurements, the output voltage remains above 2.7V up to IOH = -13.94mA. Despite this, operating beyond the recommended IOH may not guarantee reliable operation, so the largest value is -0.4mA as per the datasheet.

- c) Estimate the Thevenin equivalent: open-circuit voltage (VOC), short-circuit current (ISC), and equivalent resistance (RTH).

- Open-Circuit Voltage (VOC): 4.9V (VOH when IOH = 0)

- Short-Circuit Current (ISC): Approximate using the smallest VOH and largest IOH:

ISC ≈ VOH / R_load when R_load is smallest.

With R_load = 100Ω, ISC ≈ 4.00V / 100Ω = 40mA (negative value indicates sourcing)

- Equivalent Resistance (RTH):

RTH = VOC / ISC = 4.9V / 40mA = 122.5Ω

3. Pull-Up Configuration

- Procedure:

- We configured the DUT to output a low logic level by setting both inputs high.

- VCC was maintained at 4.75V.

- The same set of resistors was connected between the DUT output and VCC (pull-up configuration).

- For each resistor, we measured the output voltage (VOL) and calculated the output current (IOL).

- Calculations:

- IOL = (VCC - VOL) / R_load

- Current is considered positive when sinking (flowing into the output pin).

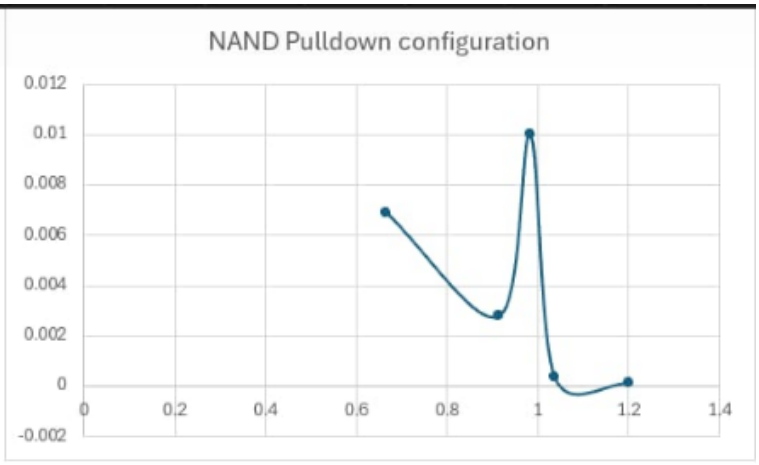
- Results:

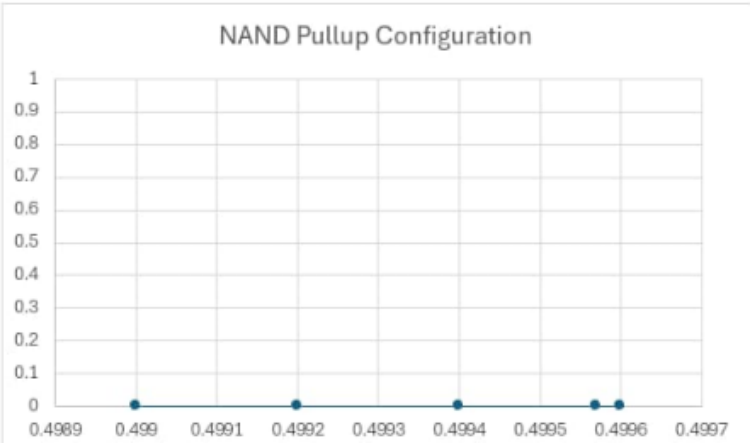
Acc	Vcc	A	B	Y	Resistor(ohms)	calc output current	measured current
0.8mA	499.5mV	499.5mV	499.5mV	499mV	9.87k	0mA	0mA
0.8mA	499.5mV	499.5mV	499.5mV	499.2mV	3.257k	0mA	0mA
0.8mA	499.5mV	499.5mV	499.5mV	499.4mV	0.9853k	0mA	0mA
0.8mA	499.5mV	499.5mV	499.5mV	499.5mV	328.21	0mA	0mA
0.8mA	499.5mV	499.5mV	499.5mV	499.6mV	97.57	0mA	0mA

- Graph:

OV (V)	OC (A)
1.201	0.0001
1.038	0.0003
0.9835	0.01
0.9151	0.0028
0.6675	0.0068

OV (V)	OC(A)
0.499	0
0.4992	0
0.4994	0
0.4996	0
0.4996	0





4. Analysis

- a) When IOL is at the maximum recommended operating condition (8mA), what is the output voltage? Does it meet the specifications for a valid logic '0'?

- Answer: At IOL = 8mA, we interpolate between the data points. Since VOL remains at 0.1V up to IOL = 46.5mA, the output voltage at 8mA is also 0.1V, which is below the maximum VOL of 0.5V. Yes, it meets the specifications for a valid logic '0'.

- b) What is the upper limit of IOL to still have a valid output voltage?

- Answer: While VOL remains within specification even at higher currents, the recommended maximum IOL is 8mA. Therefore, 8mA is the upper limit to ensure reliable operation without exceeding the device's ratings.

Part 3 – Comparison of Performance at Higher Speed

1. Building the Timing Measurement Circuit

- Procedure:

- We constructed the circuit shown in Figure 5, using three NAND gates in series before the DUT to sharpen the input signal.

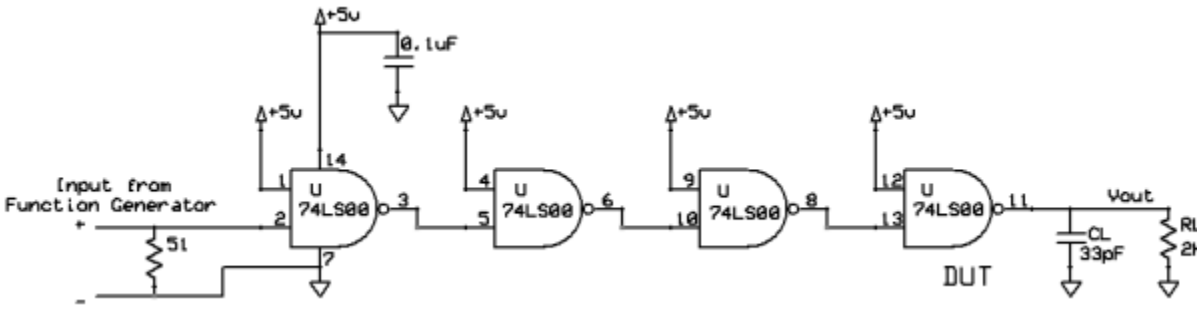
- A 2KΩ resistor (RL) and a 47pF capacitor (CL) were connected at the DUT output.

- All connections were made with the shortest possible wires, kept close to the breadboard to minimize inductance and capacitance.

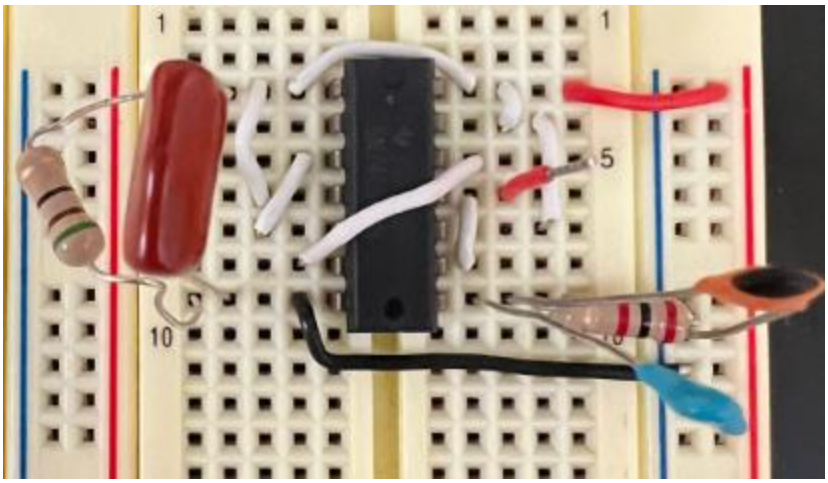
- A 0.1µF decoupling capacitor was placed across VCC and GND near the IC.

- Schematic Diagram:

- schematic diagram of the timing measurement circuit



- picture of the physical circuit, showing the short wiring and component placement.



2. Function Generator Setup

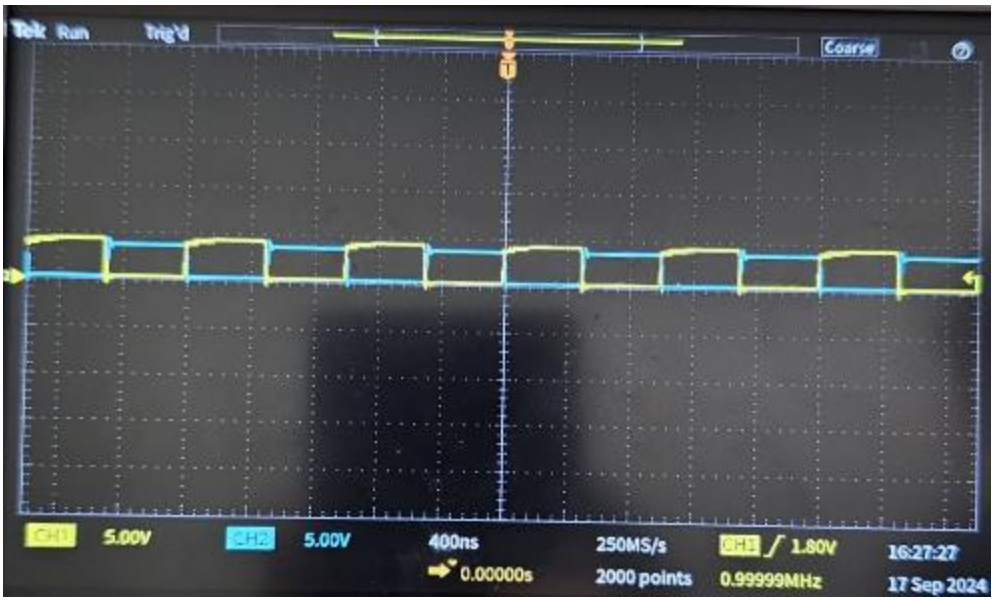
- Procedure:

- We set the function generator to output a 5V peak-to-peak, 50% duty cycle square wave at 1MHz frequency.

- The signal levels were adjusted to ensure 0V (low) and 5V (high) logic levels.

- Waveform:

- We take note of the over all wave:



3. Oscilloscope Measurements

- Equipment:

- A dual-trace oscilloscope with 500MHz bandwidth and properly compensated X10 probes was used.

- Measurement of Rise Time and tPLH:

- Procedure:

- Channel 1 was connected to the input of the DUT, and Channel 2 to the output.

- The oscilloscope was triggered on the rising edge of the input signal.

- We expanded the time scale to clearly observe the rising edge of the output signal.

- Results:

- Rise Time (t_rise): 6.64ns (from 10% to 90% of the output voltage swing).

- Propagation Delay (tPLH): 7.74ns (from 50% of input rising edge to 50% of output rising edge).

- Measurement of Fall Time and tPHL:

- Procedure:

- The oscilloscope was set to trigger on the falling edge of the input signal.

- The time scale was adjusted to observe the falling edge of the output signal.

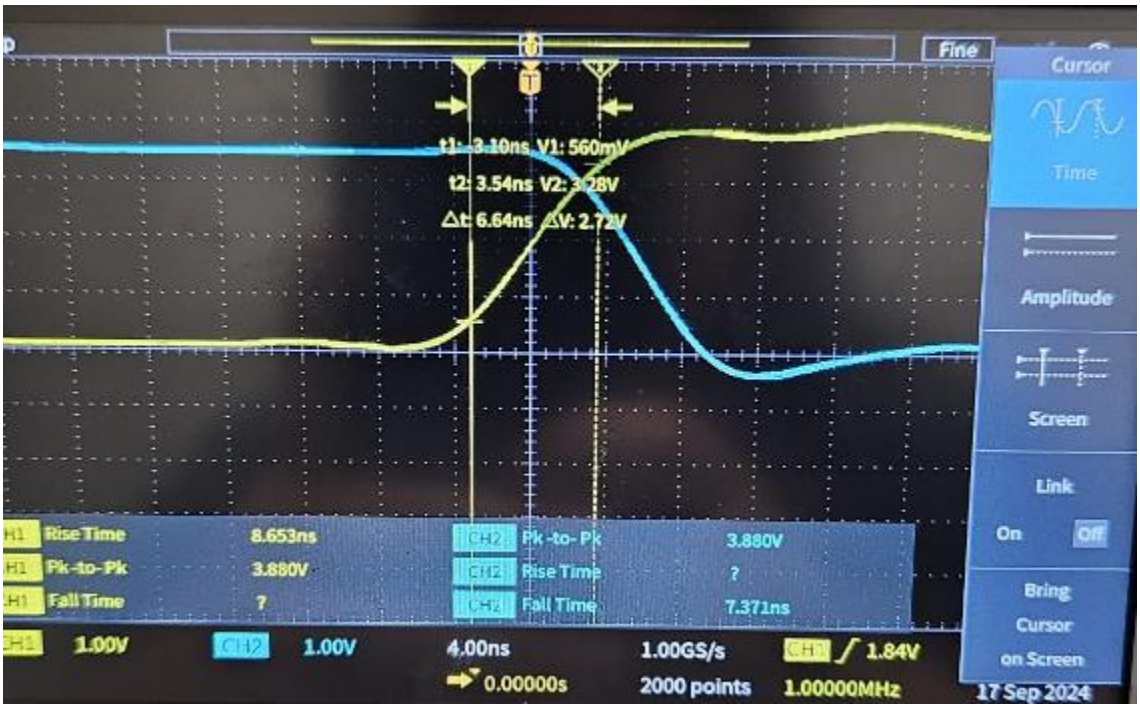
- Results:

- Fall Time (t_fall): 5.92ns (from 90% to 10% of the output voltage swing).

- Propagation Delay (tPHL): 6.26ns (from 50% of input falling edge to 50% of output falling edge).

- Waveforms:

We measure the rise time:



We measure the fall time:

- We measure the tPLH:

- We measure the tPHL:

4. Analysis

- Conclusion:

- The measured propagation delays are slightly less than the datasheet typical values but are within expected variations.

- The DUT is performing within specifications.

After Lab Questions

1. Would reversing the VOH and VIH values be acceptable?

- Answer: No, reversing the values would not be acceptable. If the chip outputted a minimum of 2.0V for a high but required at least 2.7V for a high input, the output high voltage would not be sufficient to be recognized as a valid high by another gate. This mismatch would lead to logic errors, as the output of one gate would fail to drive the input of the next stage properly.

2. Why did Fairchild Semiconductor choose to measure input currents with VCC = VCC(max) and output voltages with VCC = VCC(min)?

- Answer: Measuring input currents at VCC(max) and output voltages at VCC(min) tests the device under worst-case conditions. At VCC(max), the voltage difference across the input is greatest, potentially leading to higher input currents. Testing here ensures the input currents remain within specified limits under maximum stress. Similarly, measuring output voltages at VCC(min) verifies that even at the lowest supply voltage, the device can still produce valid logic levels, ensuring reliable operation across the entire supply voltage range.

Conclusion

Through this lab, we gained practical experience in testing and analyzing the non-ideal behaviors of logic gates. We observed how output voltages vary with different input voltages and loading conditions, and how the gates perform at higher speeds. By comparing our practical measurements with theoretical and simulated results, we confirmed that the 74LS00 NAND gate operates within the manufacturer's specifications under various conditions. This understanding is crucial in designing reliable digital circuits that function correctly in real-world applications.

IV. CONCLUSIONS

In this experiment, the primary objectives of testing non-ideal logic components were met, providing insights into the performance and limitations of the 74LS00 NAND gate. Through a series of tests, we determined the valid input voltage ranges, output voltage behavior under various loads, and timing characteristics.

The findings revealed that while the device generally functioned within the specifications outlined in its datasheet, certain discrepancies were noted between theoretical predictions, practical results, and simulation outcomes. For instance, the actual output voltages at high and low states did not always align perfectly with the ideal 5V and 0V, respectively, particularly under load conditions. This deviation highlights the non-ideal nature of the logic gates and emphasizes the importance of considering real-world factors like output current and load resistance in circuit design.

The significance of these results reinforces the hypothesis that non-ideal characteristics significantly affect logic gate performance. Understanding these limitations is crucial for engineers, especially when designing circuits that rely on precise logic levels.

However, several limitations were identified during the experiment. The reliance on specific resistor values for load testing may have introduced errors, particularly if the resistors deviated from their specified tolerances. Additionally, variations in measurement techniques, particularly with the oscilloscope, could impact rise and fall time measurements, which are critical for high-speed applications.

Future investigations could explore a broader range of logic gates and configurations to assess how different logic families behave under similar conditions. Additionally, studying the effects of temperature and supply voltage variations on logic performance could provide further insights into the robustness of digital circuits. Advanced simulations could also be employed to predict performance more accurately and validate experimental findings.

Overall, the lab successfully illuminated the complexities involved in working with non-ideal logic components, underscoring the necessity of thorough testing and analysis in electrical engineering practices. Future work could explore the performance of different logic families or incorporate additional variables, such as temperature effects, to further deepen our understanding of logic gate behavior.

The University of Texas Rio Grande Valley
Electrical & Computer Engineering
Lab Demonstration Certification

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This section to be filled in by the project team.

Course: EECE 3225 Experiment: Lab 2

Team Members:
1. Jesay Garcia Quezada
2. Enrique Casiano
3. Jordan Lara

Describe what is being demonstrated:

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This section is to be filled in by instructor.

Signature:	Date:	Time:
	9/17/2024	

Comments:

If an instructor is not available at demo time, this form can be signed by an EECE faculty or teaching assistant.
Include this certification in the lab report.